Lab 3:

Embedding VHDL code in a Xilinx Spartan 3E VI

Keywords: LabVIEW, LabVIEW FPGA, Xilinx SPARTAN3E Starter Kit, VHDL, Even Parity.

Introduction

Welcome to Lab3 in the serie of programming a SPARTAN3E Starter Kit by use of LabVIEW FPGA. These labs are created by Vincent Claes. If you encounter problems using this labs or want some advice/consultancy on LabVIEW and especially LabVIEW FPGA you can always contact the author.

These labs are free to use however to show respect to the author please email him when you use them with your contact details (feedback is also welcome).

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Software Requirements:

- LabVIEW 8.5 or above
- LabVIEW 8.5 FPGA module
- XUP Spartan3E starter board: download for free from: https://lumen.ni.com/nicif/us/infolvfpgaxilsprtn/content.xhtml

Hardware Requirements:

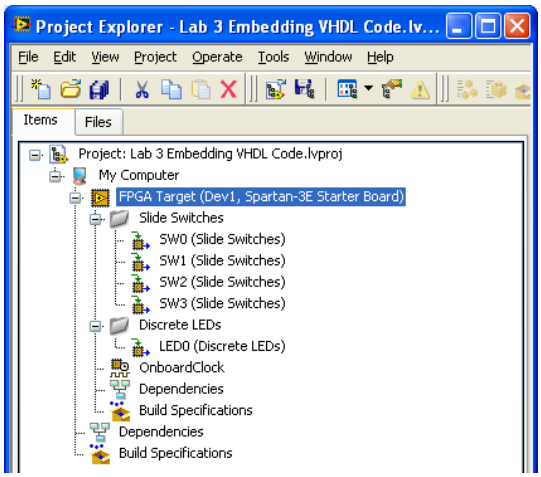
- Xilinx Spartan3E Starter kit: http://www.xilinx.com/products/devkits/HW-SPAR3E-SK-US-G.htm
- User manual: www.xilinx.com/support/documentation/boards_and_kits/ug230.pdf

Getting Started

When you want to use this labs you have to setup your board. This labs are written for the Xilinx SPARTAN3E Starter Kit so it is quite interesting to read the user manual of the board. Be sure to plug in the USB cable, plug in the Power cord and Switch the board on before starting the lab.

Step 1: Adding the FPGA I/O to your LabVIEW FPGA Project

The first things we have skipped because it is the same as in Lab 1 & Lab 2. Try to setup yourself an LabVIEW FPGA project for the Xilinx Spartan3E starter board. When you reach the step where you have to add FPGA I/O to the FPGA Project add the "SW0", "SW1", "SW2", "SW3" and "LED0" I/O pins.

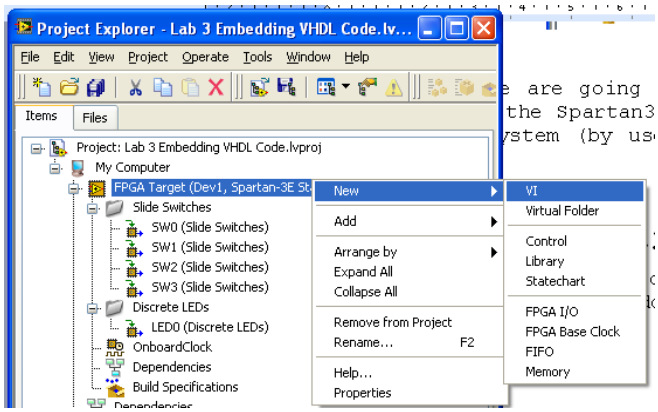


In this lab we are going to create a parity checker. We will put "LED0" of the Spartan3E Starter board on when the input of the checker system (by use of "SW0", "SW1", "SW2" and "SW3") has even bits.

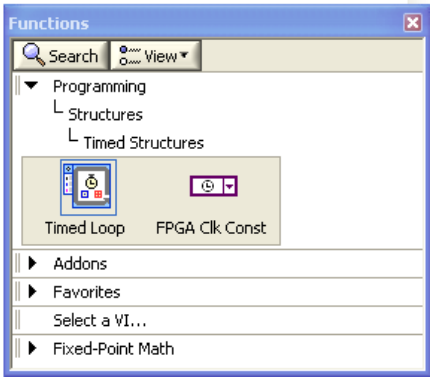
Step 2: Creating the VI.

Do a "right mouse click" on the "FPGA Target" in the "Project Explorer". From the pull down menu select "New" >> "VI".

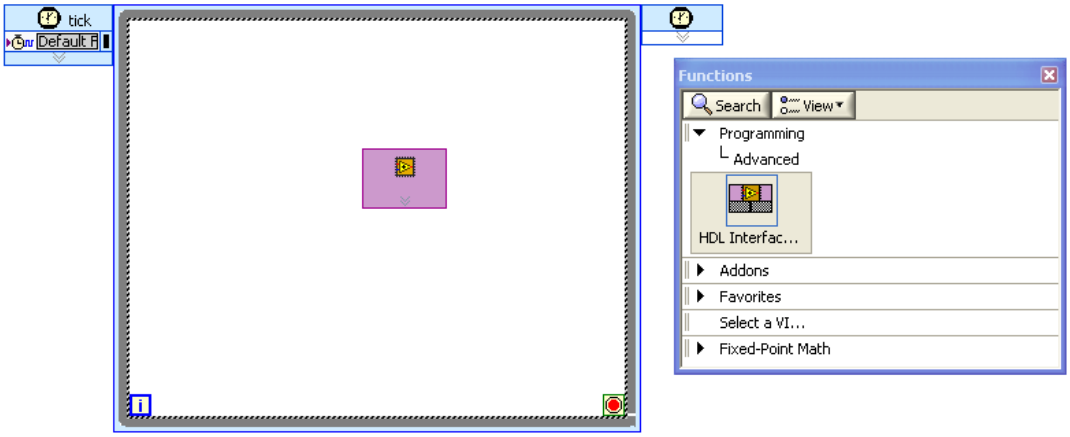
Name it "FPGA_VI_VHDL".



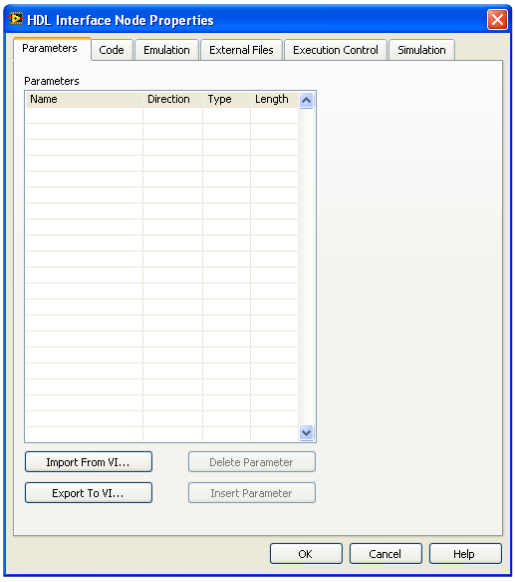
On the "block diagram" of this vi you have to put a "Timed Loop".



In this "Timed Loop" you have to place a "HDL Interface Node".

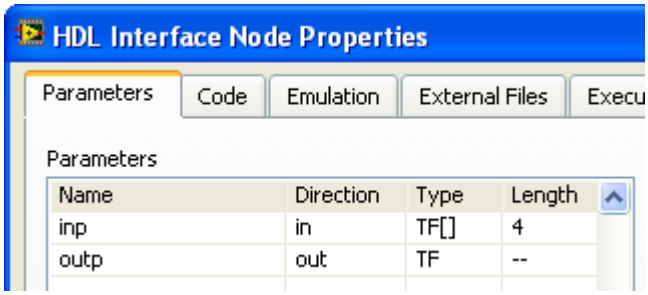


Now double click the "HDL Node"; you will get the following screen:



In the first screen try to add the following 2 parameters:

- "inp" with direction "in", type "TF[]" and Length "4".
- "outp" with direction "out" type "TF".



In the code screen replace “hdlnode” (name of the entity) to “even_parity”.

The field below “architecture implementation of even_parity is” has to been filled with the following VHDL rule:

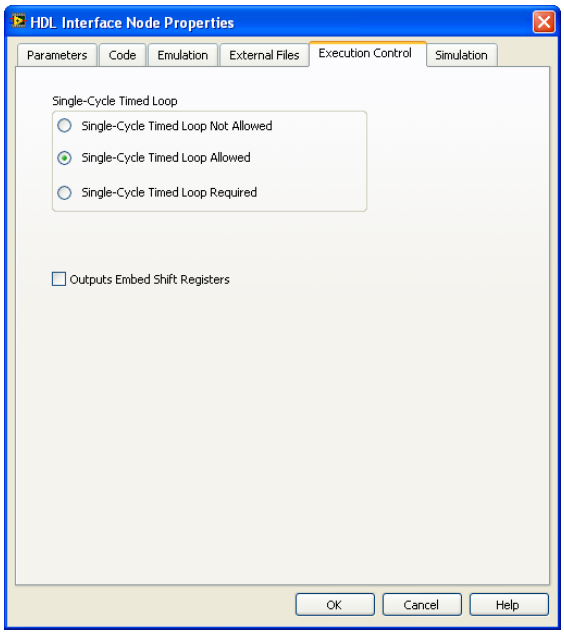
```
signal s1, s2, s3, s4, s5, s6, s7, s8: std_logic;
```

The field below the VHDL keyword “begin” has to been filled with the following VHDL code:

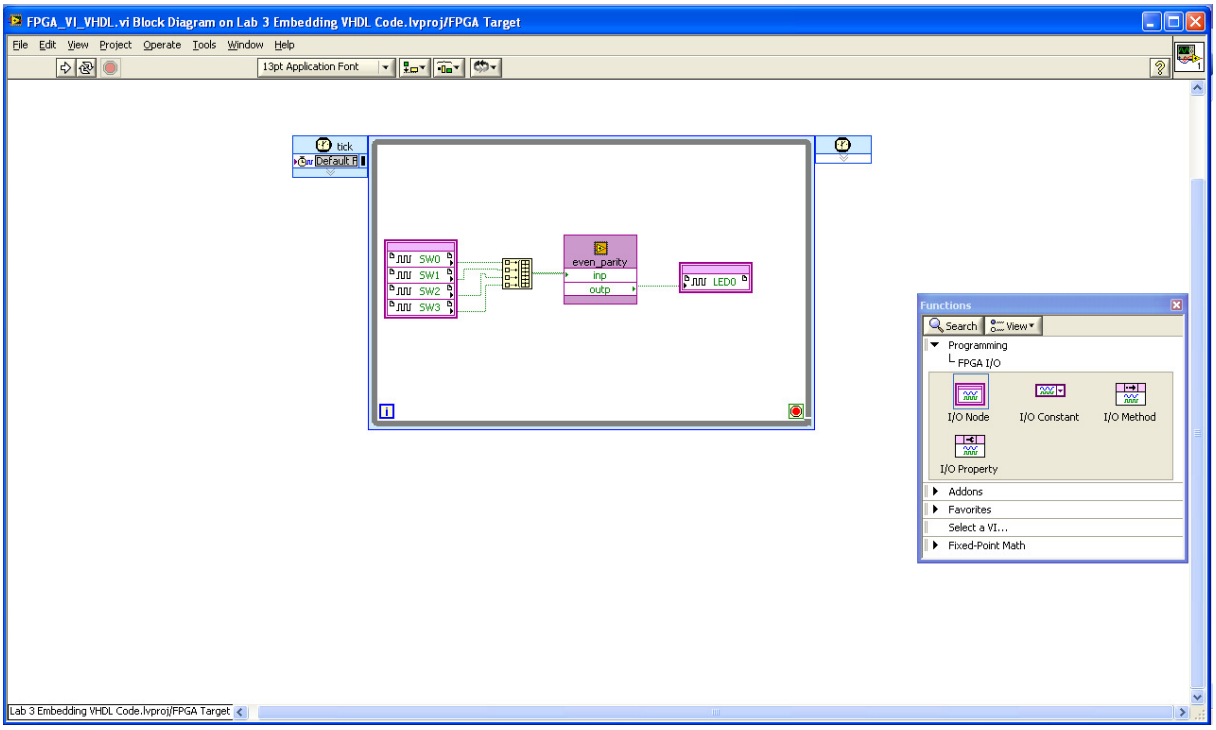
```
outp(0)<=((s1 or s2) or (s3 or s4)) or ((s5 or s6) or (s7 or s8));
s1       <=(not inp(3)) and (not inp(2)) and (not inp(1)) and (not inp(0));
s2       <=(not inp(3)) and (not inp(2)) and inp(1) and inp(0);
s3       <=(not inp(3)) and inp(2) and (not inp(1)) and inp(0);
s4       <=(not inp(3)) and inp(2) and inp(1) and (not inp(0));
s5       <=inp(3) and (not inp(2)) and (not inp(1)) and inp(0);
s6       <=inp(3) and (not inp(2)) and inp(1) and (not inp(0));
s7       <=inp(3) and inp(2) and (not inp(1)) and (not inp(0));
s8       <=inp(3) and inp(2) and inp(1) and inp(0);
enable_out<='1';
```

This is a very simple VHDL program to show you how you can add VHDL code to your Spartan3E LabVIEW FPGA project.

In the tab “Execution Control” check the option “Single-Cycle Timed Loop Allowed” and click the “OK” button.

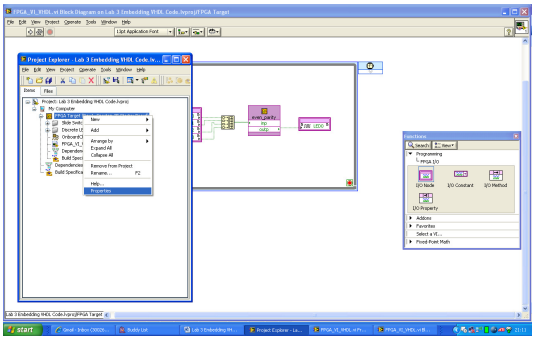


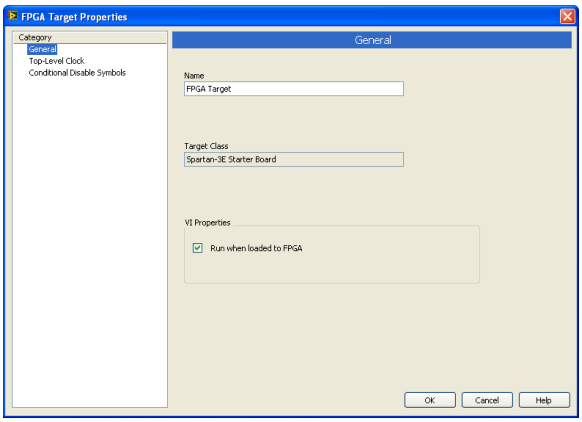
Now place two “FPGA I/O Node’s” on the block diagram of your vi. Build an array with “SW0”, “SW1”, “SW2” and “SW3” as inputs. Connect the output of this “build array” function to the input of the “HDLNode” called “inp”. Connect now “LED0” to “outp” of the “HDLNode”.



Step 3: Running the VI.

Now go to the “Project Explorer”. Right mouse click on “FPGA Target” then select “Properties”.

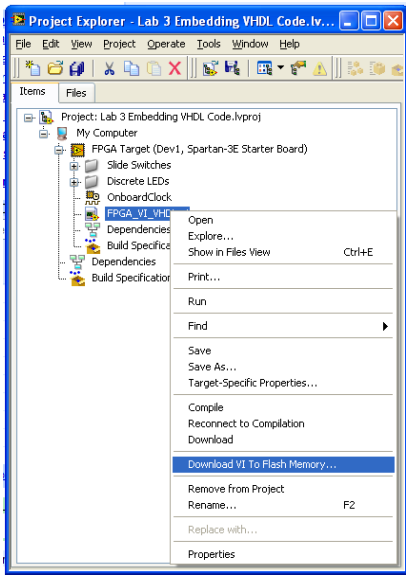




Be sure to check in this window “Run when loaded to FPGA” before compiling the vi.

Go back to “Project Explorer”. Do a right mouse click on “FPGA_VI_VHDL”. Select Compiler and let the LabVIEW FPGA code compile.

When the compilation completed go to “Project Explorer” and do a right mouse click on “FPGA_VI_VHDL” and select “Download VI to Flash Memory”



When the download completed push the "reset" button on the Xilinx Spartan3E board and the application should run.

Enjoy.

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