



## **Lab 1:**

### **Implementing a Boolean function in LabVIEW FPGA on the Xilinx SPARTAN-3E Board**

Keywords: LabVIEW, LabVIEW FPGA, Xilinx SPARTAN3E Starter Kit,  
Implementing a Boolean Function.

# Introduction

Welcome to Lab1 in the serie of programming a SPARTAN3E Starter Kit by use of LabVIEW FPGA. These labs are created by Vincent Claes. If you encounter problems using this labs or want some advice/consultancy on LabVIEW and especially LabVIEW FPGA you can always contact the author.

These labs are free to use however to show respect to the author please email him when you use them with your contact details (feedback is also welcome).

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## **Software Requirements:**

- LabVIEW 8.5 or above
- LabVIEW 8.5 FPGA module
- XUP Spartan3E starter board: download for free from:  
<https://lumen.ni.com/nicif/us/infolvfpgaxilsptrn/content.xhtml>

## **Hardware Requirements:**

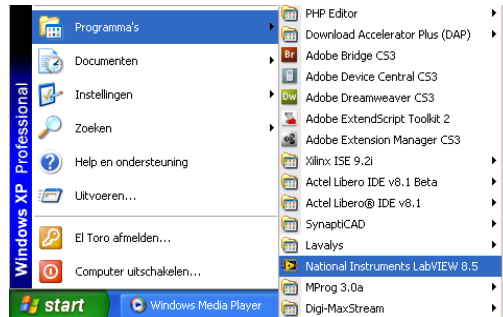
- Xilinx Spartan3E Starter kit:  
<http://www.xilinx.com/products/devkits/HW-SPAR3E-SK-US-G.htm>
- User manual:  
[www.xilinx.com/support/documentation/boards\\_and\\_kits/ug230.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ug230.pdf)

# Getting Started

When you want to use this labs you have to setup your board. This labs are written for the Xilinx SPARTAN3E Starter Kit so it is quite interesting to read the user manual of the board. Be sure to plug in the USB cable, plug in the Power cord and Switch the board on before starting the lab.

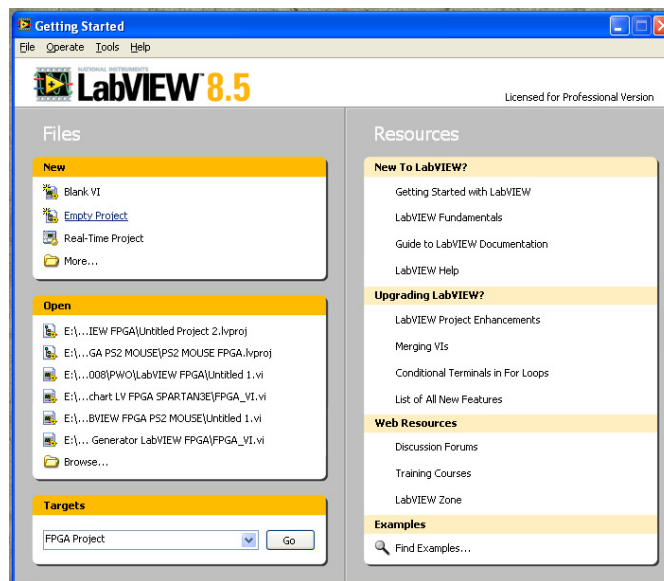
# Step 1: Starting LabVIEW

The first step is to start the National Instruments LabVIEW 8.5 environment.



# Step 2: Create a LabVIEW project

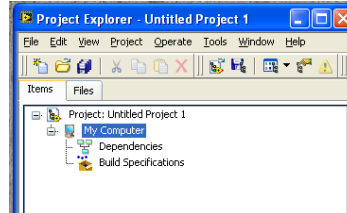
After we have started the LabVIEW environment we get the following screen:



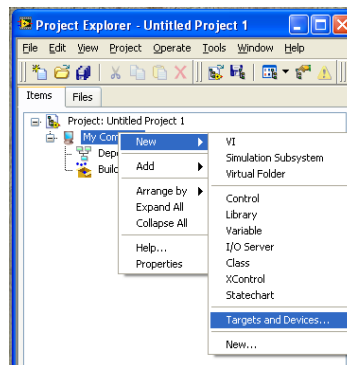
We have to create an Empty Project where we will add the Xilinx Spartan3E starter board on as a hardware target. In a future lab I will explain how we can create a HOST vi (this is a LabVIEW application that runs on a desktop PC) that communicates with a LabVIEW FPGA vi.

## Step 3: Add the Spartan3E board as a hardware target

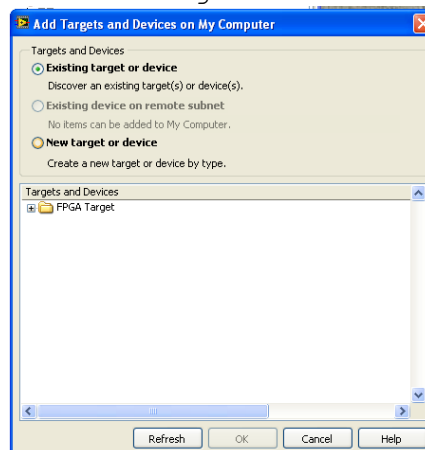
The next screen shows the Project Explorer view of the Empty Project that we just created.



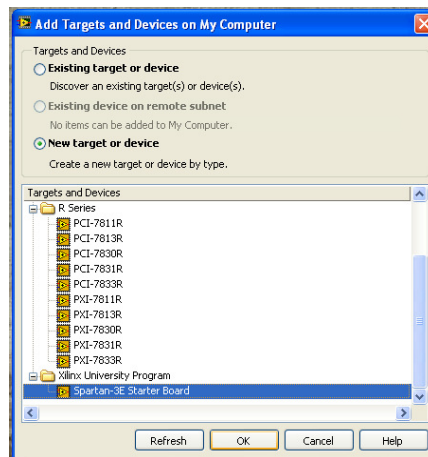
Now we have to add the Spartan3E starter board as a Hardware target. For this we do a "right click" on "My Computer" in the Project Explorer view. We select "New" and then "Targets and Devices".



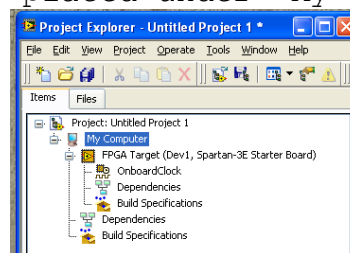
In the screen that now appears we have to select the XUP starter board. Select "New target or device".



A list of "Targets and Devices" will be shown. You have to scroll down till the end and select "Spartan-3E Starter board" from the "Xilinx university Program" map.

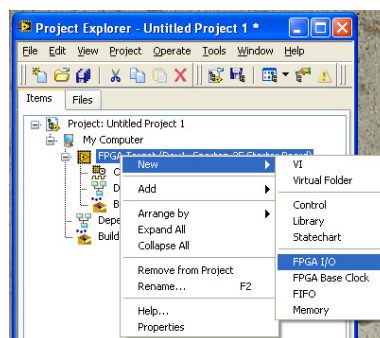


This will add the FPGA Target to the Project Explorer view. You see this target is placed under “My Computer”.

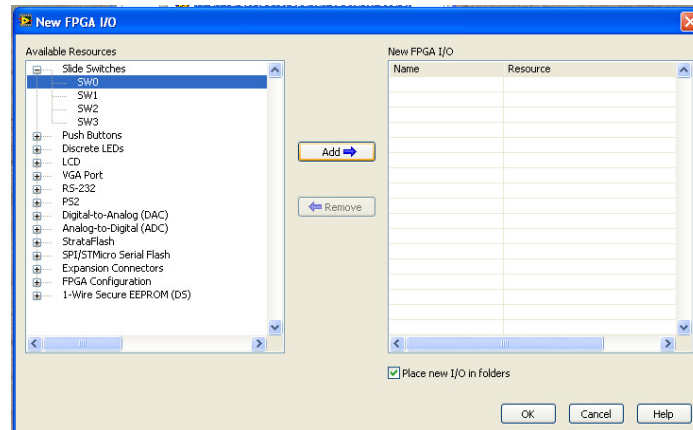


## Step 4: Adding FPGA I/O

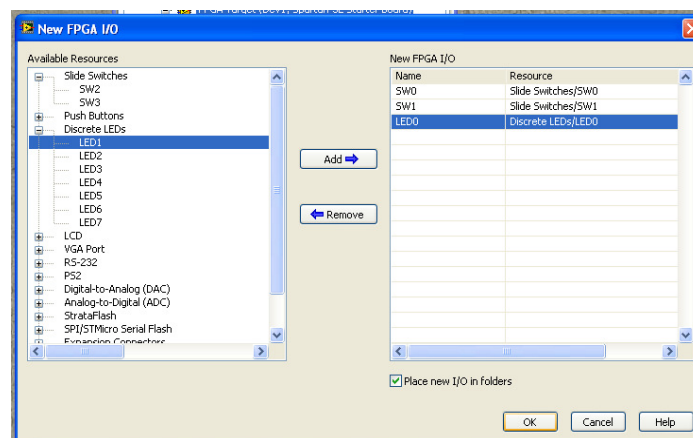
The next step we make is adding “FPGA I/O’s” that we will use in this project to the Project Explorer view. For this you have to “right click” the FPGA Target you added in Step 3. Select “New” “FPGA I/O”.



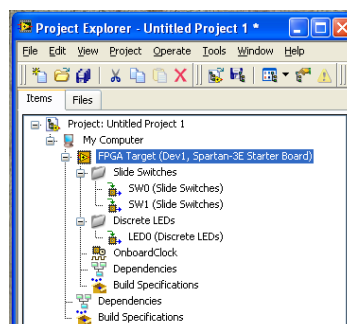
The next screen will appear



On the left side of this screen you see all the resources that are available on the Spartan-3E board. To add FPGA I/O to the project you have to select it in the left window and press the "Add" button. Now the FPGA I/O that you wanted to add has to show up in the window on the right side. For this project you have to add SW0, SW1 and LED0 to the project.



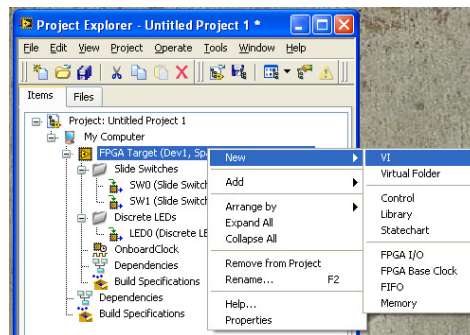
If we go back to the "Project Explorer" view we see the FPGA I/O that we have added. With this I/O we will implement an Exclusive-OR function.



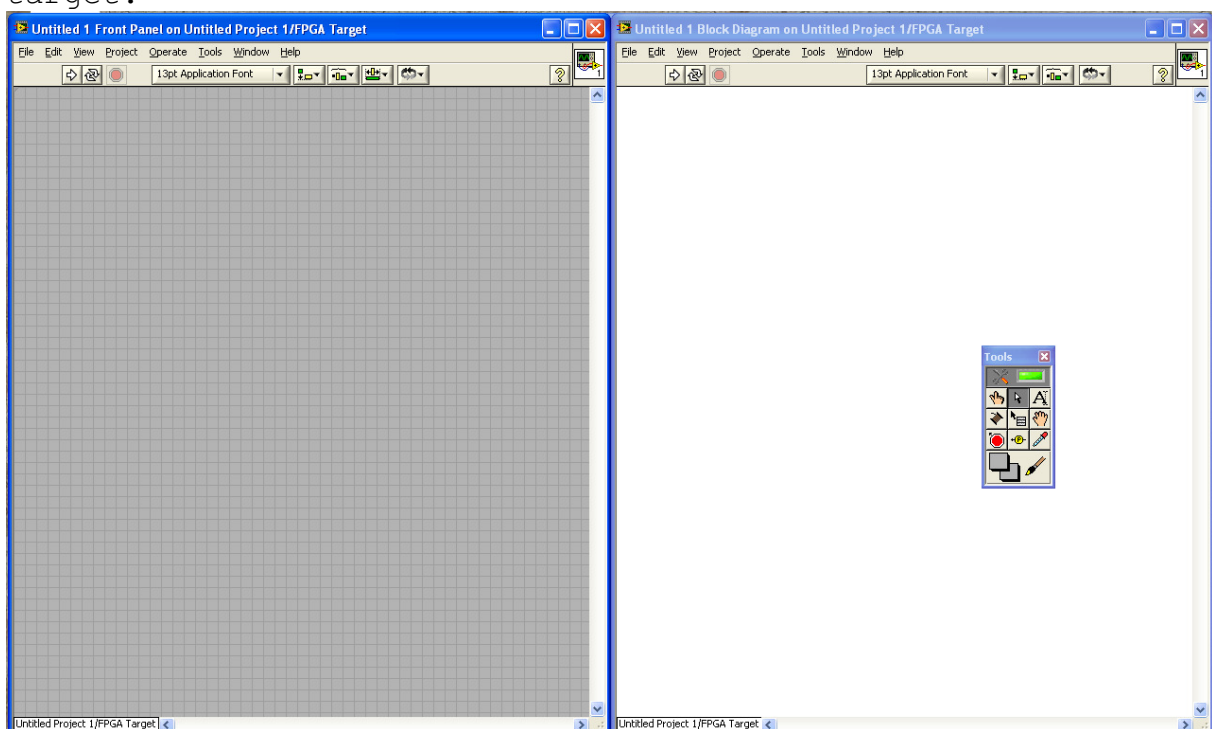
## Step 5: Creation of the FPGA VI

The next step is the creation of a hardware program that runs on the Xilinx Spartan-3E hardware target.

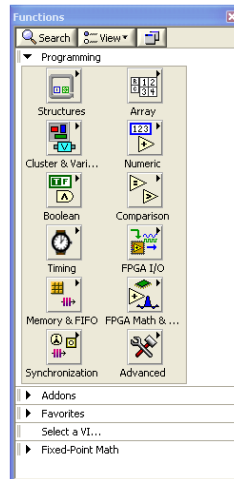
For this we do again a “right mouse click” on the FPGA target in the “Project Explorer” view. Select “New” VI. Be sure that you have right clicked the FPGA target and not “My Computer” because otherwise you will be creating a vi that runs not in Hardware (on the FPGA) but on your computer.



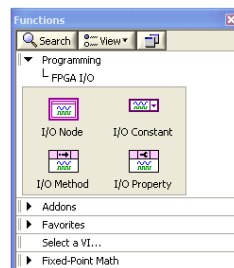
This step will open the Front Panel and Block Diagram of the FPGA VI you just started creating. The code we will be implementing is an Exclusive-OR function. The view I always use in LabVIEW is the “tile left and right” view. You can select this by going to “Window” and then selecting “Tile Left and Right”. We you did all the steps right you have to see in the left corner of either the Front Panel or Block Diagram the name of the vi you created with /FPGA target behind it. This shows that the vi you are creating is aimed at the FPGA target.



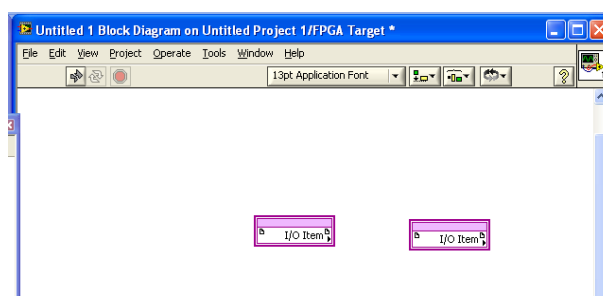
For now have a look at the “Functions Palette” which you can see when you click in the “Block Diagram” on “View” and then “Functions Palette”. You see that the available functions are different. You see “FPGA I/O”, “Memory & Fifo” and “FPGA Math & Analysis”. Those are specially for using on FPGA targets.



Click in the Functions Palette on “FPGA I/O”.

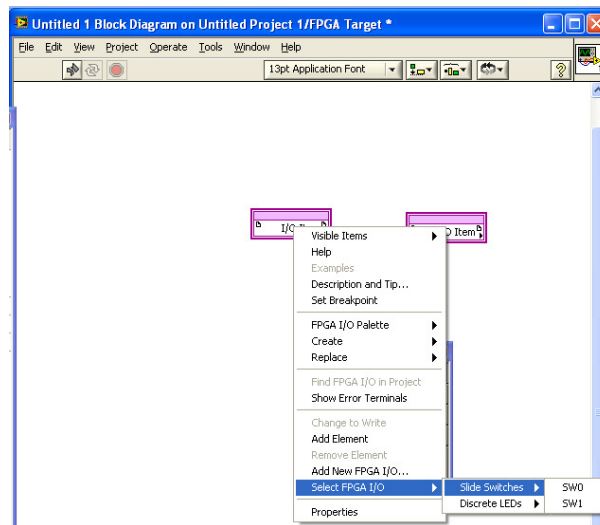


Place 2 I/O Nodes on the Block Diagram of the LabVIEW FPGA vi.

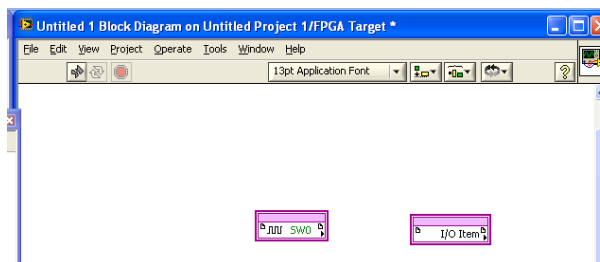




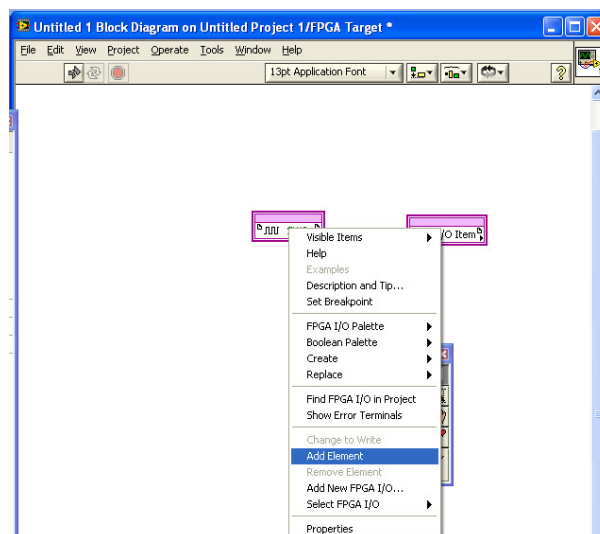
Now do a “right mouse click” on one of the I/O Nodes. Select “Select FPGA I/O” then “Slide Switches” then “SW0”.



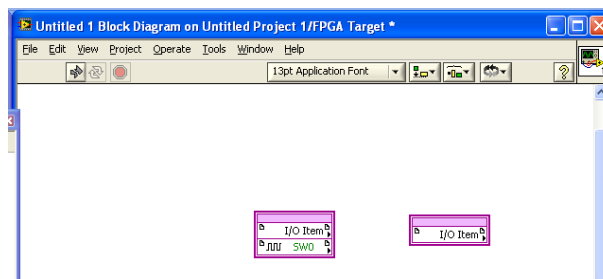
You should see that the I/O node is filled with a green “SW0” label. The color green is standing for a Boolean variable. This is correct since a slider switch can only have the value of true or false.



This project will be using 2 slider switches so we have to add another FPGA I/O. For this do a right click on the FPGA I/O you just filled with SW0. Select “Add Element”.

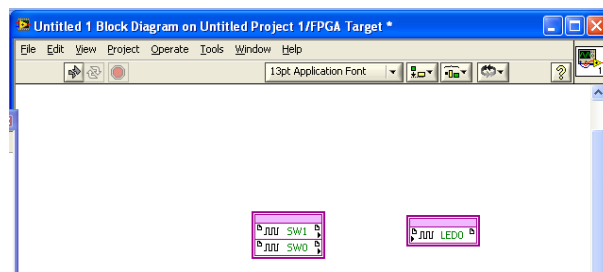


The following is the screen you should have now:

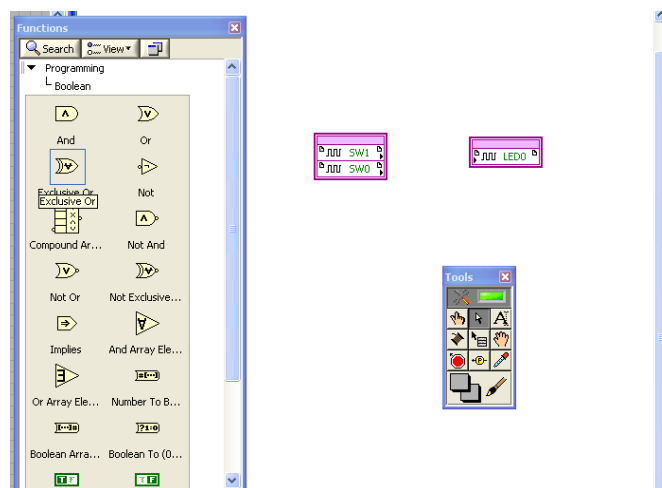


Try now to fill the I/O Item yourself with SW1. Try also to fill the I/O Node that is empty with LED0. This is done by right mouse clicking it then selecting "Select FPGA I/O". In the option of "Select FPGA I/O" you see only the resources you added in the "Project Explorer" view to the project.

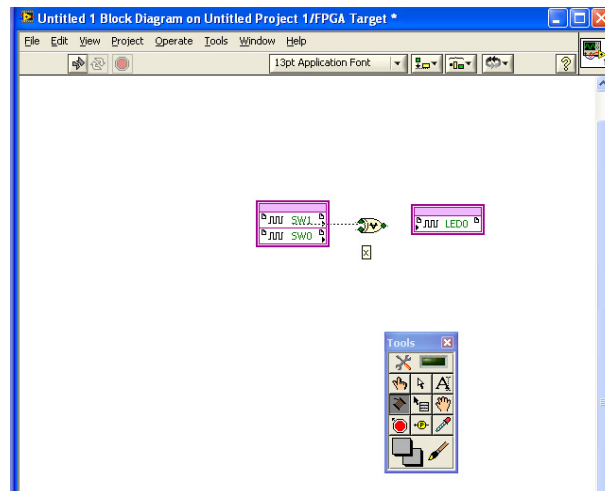
The following screen will be created:



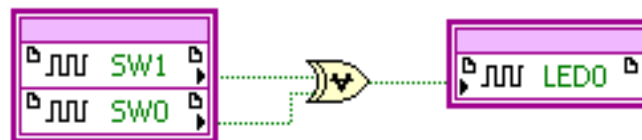
Now we will as an example implement an exclusive-OR Boolean function into the FPGA. From the "Functions Palette" select "Programming" "Boolean" and look for the "Exclusive Or" function. Place this one on the Block diagram.



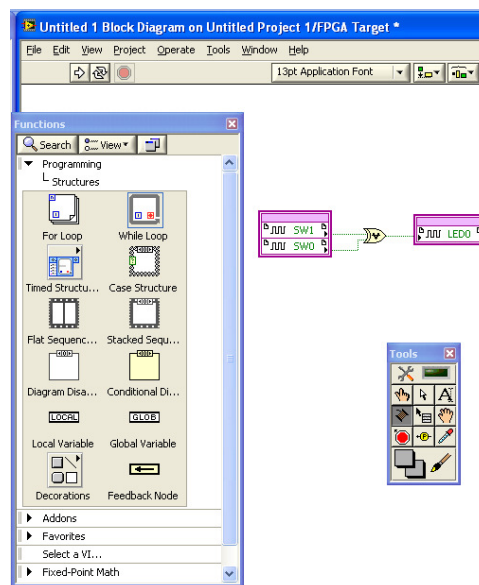
Wire the "SW1" and "SW0" FPGA I/O to the Exclusive-OR inputs. Wire the output of the function to "LED0".

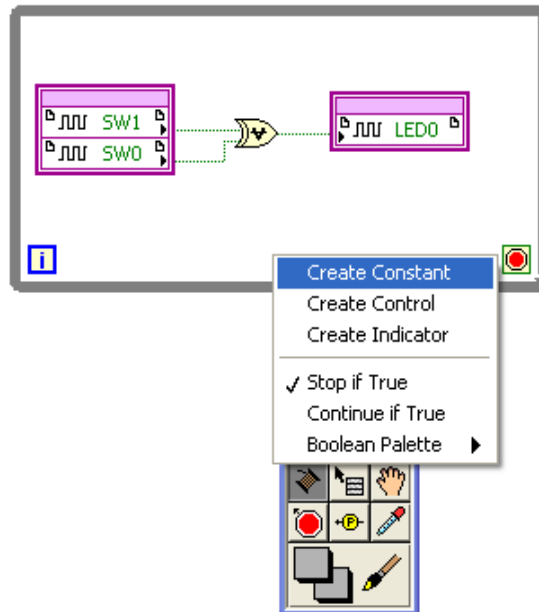


Your code has to look like this:

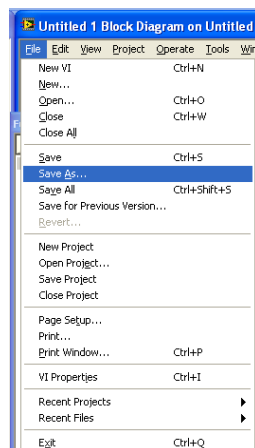


When you implement the function like presented above the function will run only once. We would like to implement it that it runs continuously. For this we place a "While Loop" around it and we wire a Boolean "False constant" to the "stop condition" of this loop. This you normally don't do on a PC because this will put your PC in a never ending loop. The "While Loop" you find on the "Functions Palette".

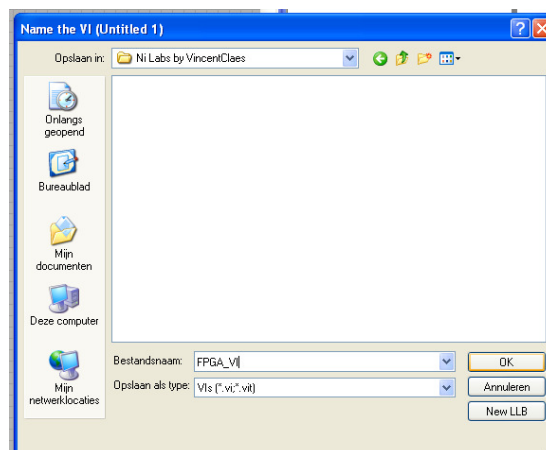




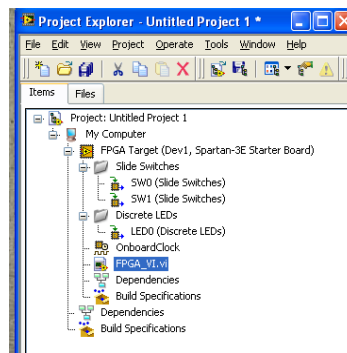
Now it is time to save your vi that you created for the FPGA. You do this by selecting “New” “Save As” in either the “Front Panel” or the “Block Diagram”.



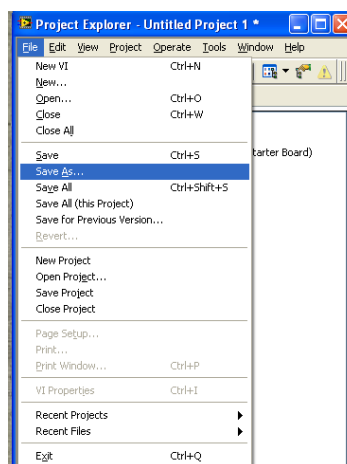
The name I usually use is FPGA\_VI for the vi running on the FPGA.



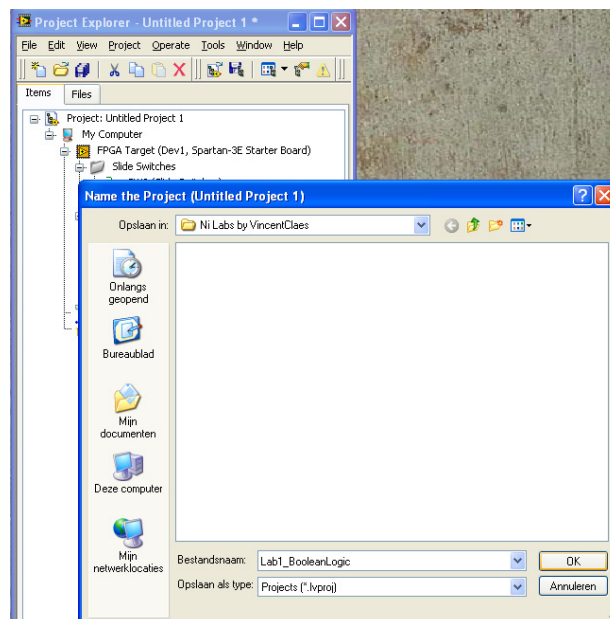
In "Project Explorer" you should see the following



It is also a good idea to save the project file for this select in the "Project Explorer" "New" then "Save As".

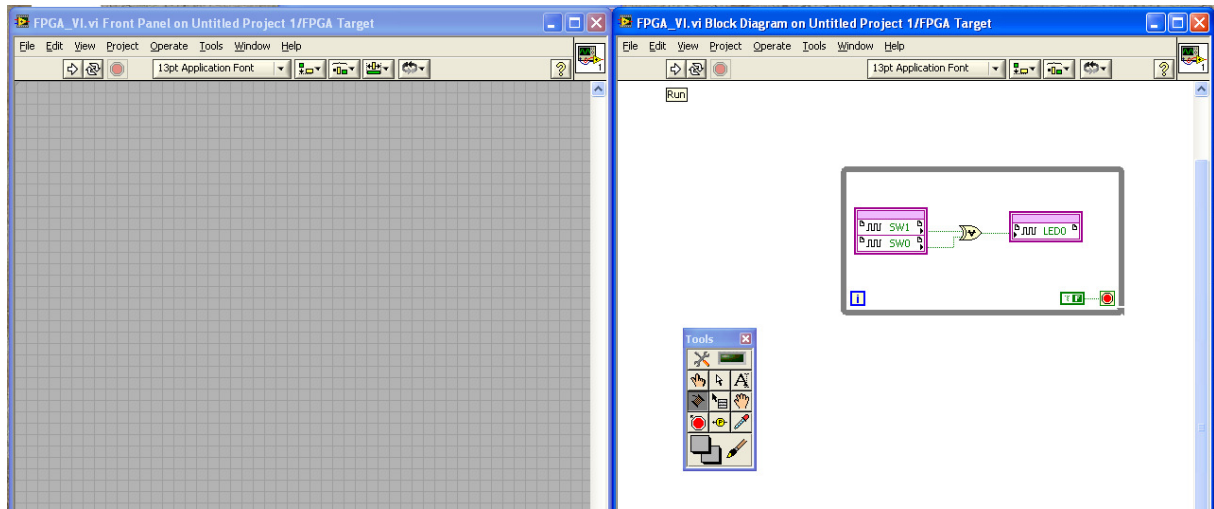


I did use the name Lab1\_BooleanLogic

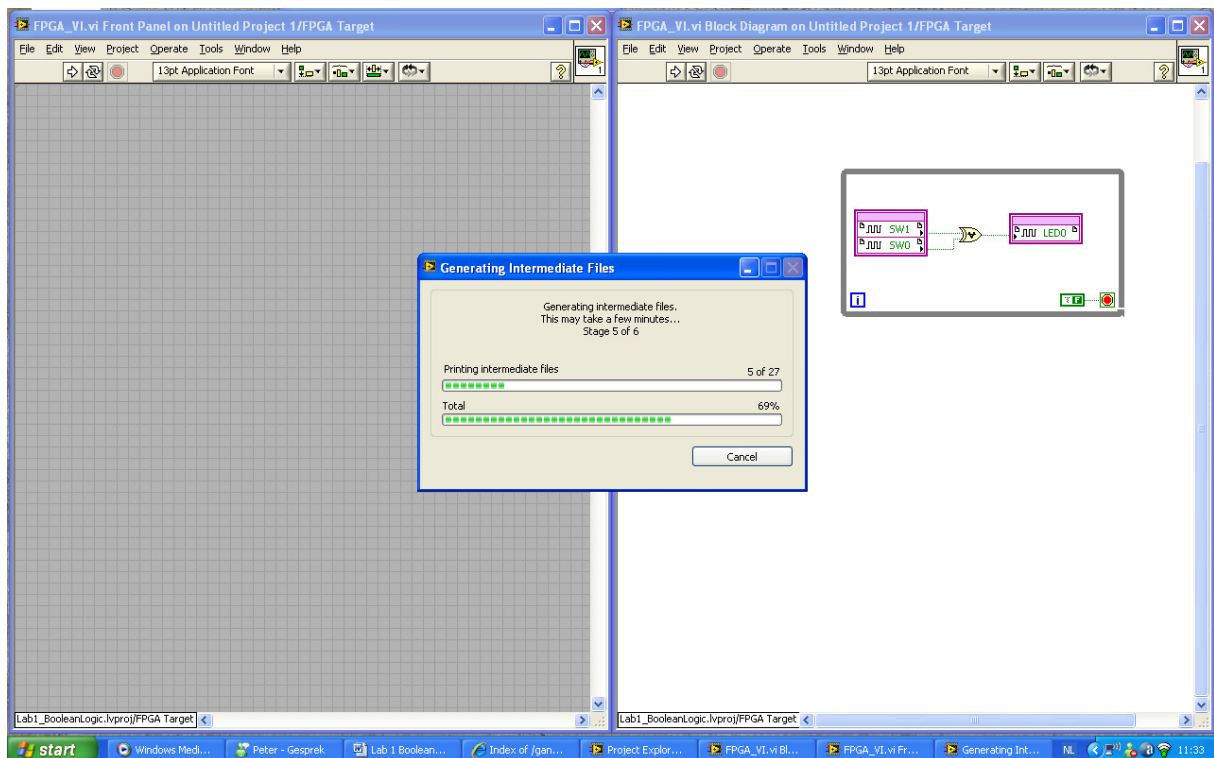


## Step 5: Running the FPGA VI

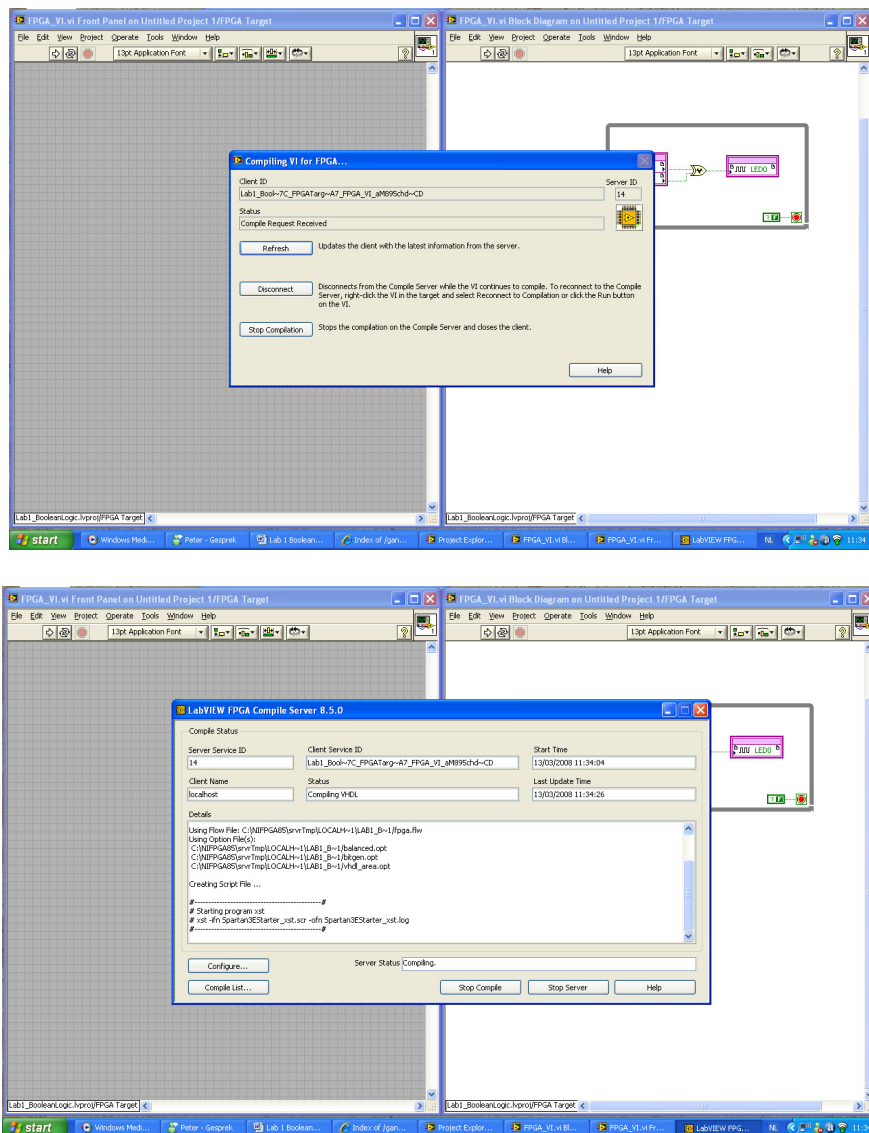
This step is where we created the vi for. We designed it to run on an target. For starting the executing of this vi we have to press the "Run" arrow on either the "Block Diagram" or on the "Front Panel".



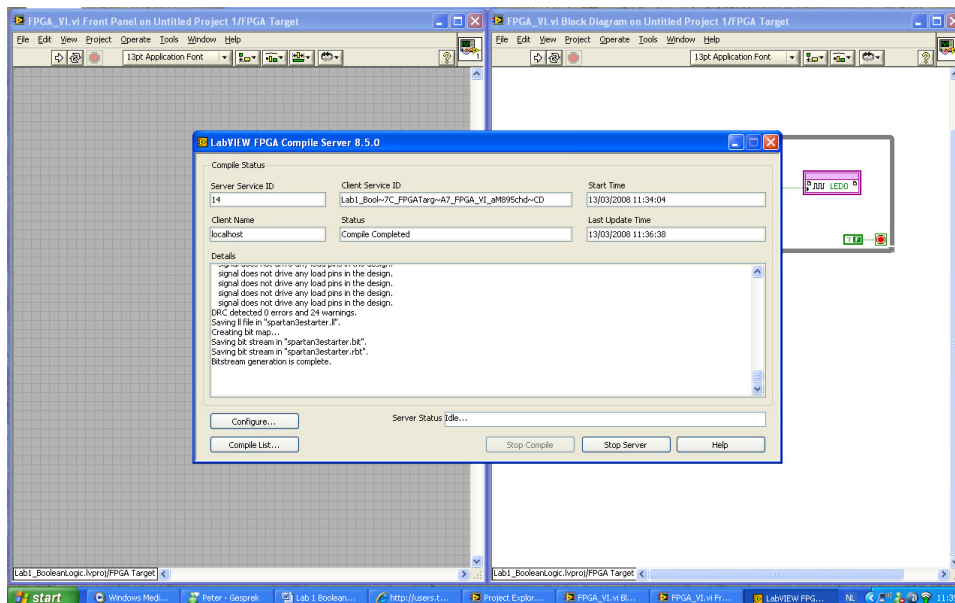
The first step LabVIEW does is "Generating Intermediate Files". This files will be send to the Xilinx Synthesis Tools. But this is not important for us as application developers.



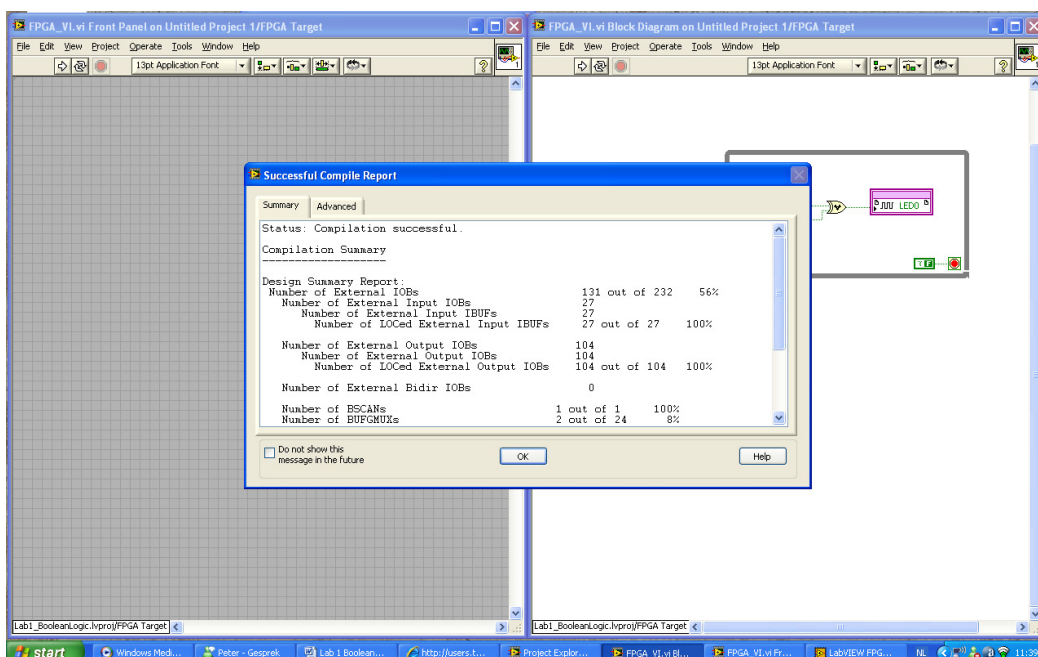
In this step you see that LabVIEW is starting the “Compile Server”. This “Compile Server” can also be executed on another “more powerful” machine that is in your network (for this please see the information on the NI website).



When the “Bitstream generation is complete” message appears and the server status is set to “Idle...” the Xilinx synthesis tools have done their job.

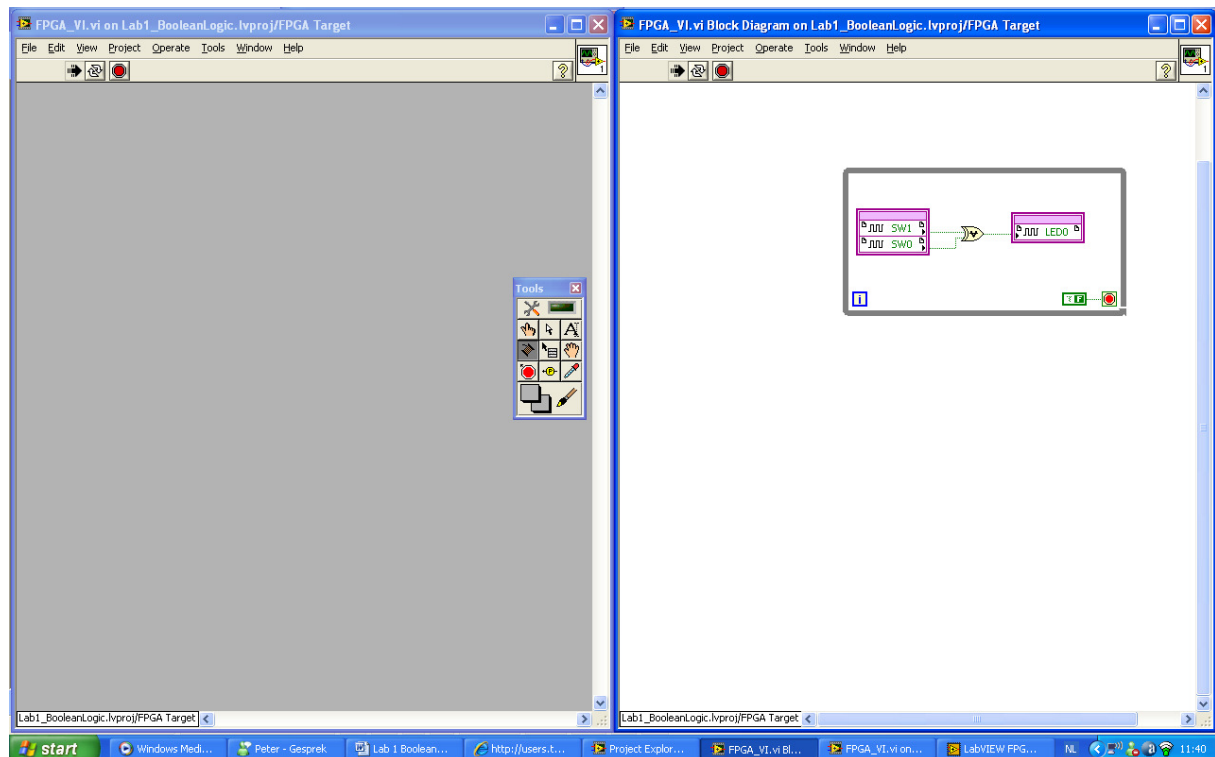


You get a “Successful Compile Report” where you can see the implementation details of your code. You have to Press “Ok”.





After you have pressed the “Ok” button your VI starts running on the FPGA target. It is indicated on your screen by the black “Run” arrow.

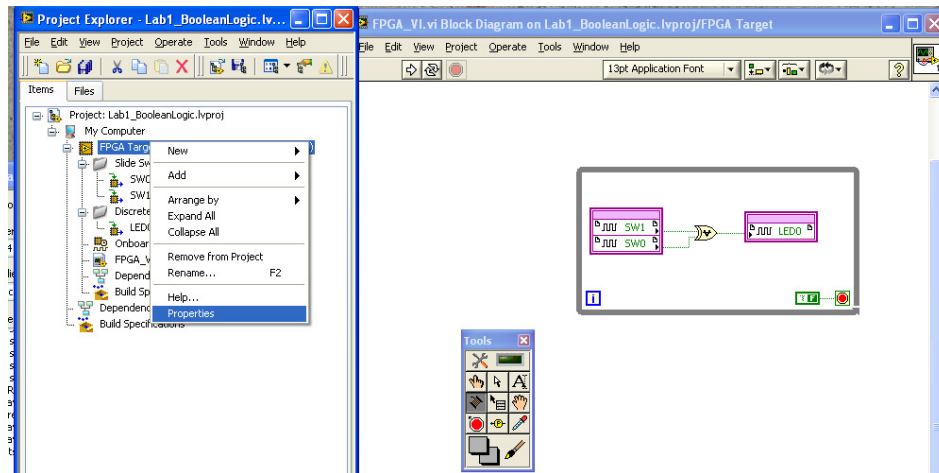


Try to play with the switches SW0 and SW1 on the Spartan3E starter board you will see they have an XOR function; the led LD0 will be on when one of those switches is turned on.

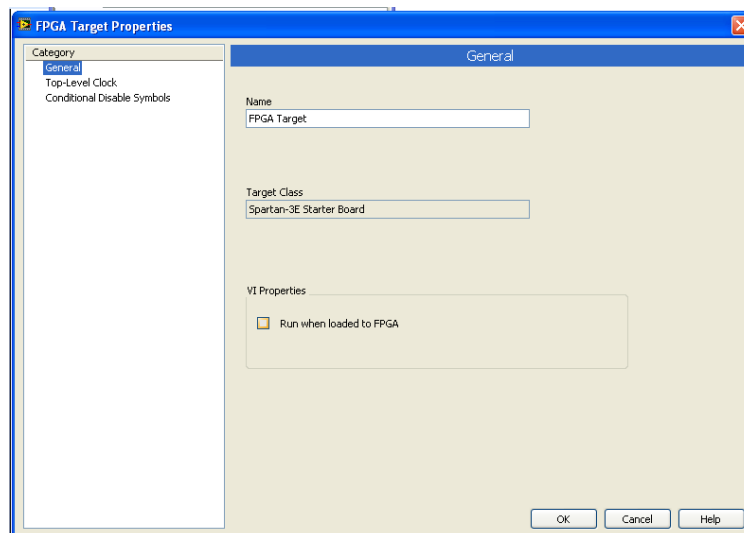
The problem with this implementation is that when you stop the VI the function is erased on the LabVIEW FPGA board. If you don't want this effect you can download this VI to the FLASH of the Xilinx Spartan3E starter board (see next step).

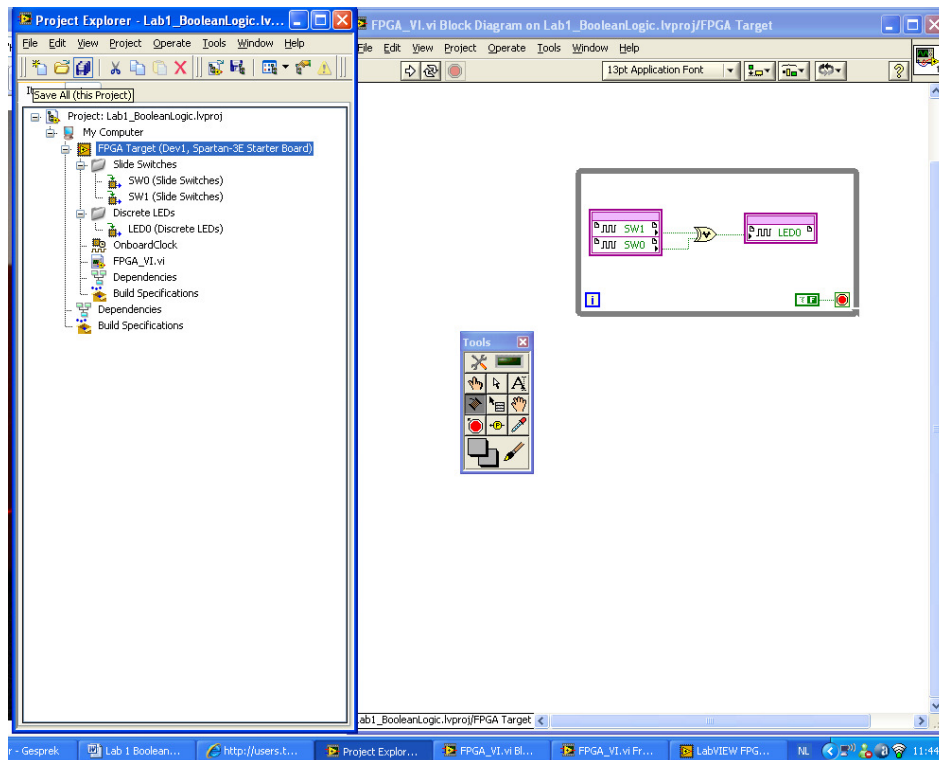
## Step 6: Implementing the LabVIEW VI into Flash

For implementing your VI into the Flash on the Spartan3E Starter board you have to do some things. The first thing is setting the option of "Run when loaded to FPGA" on. For this you have to go to "Project Explorer". Then "Right Mouse click" on your FPGA target. Select the "Properties" option.

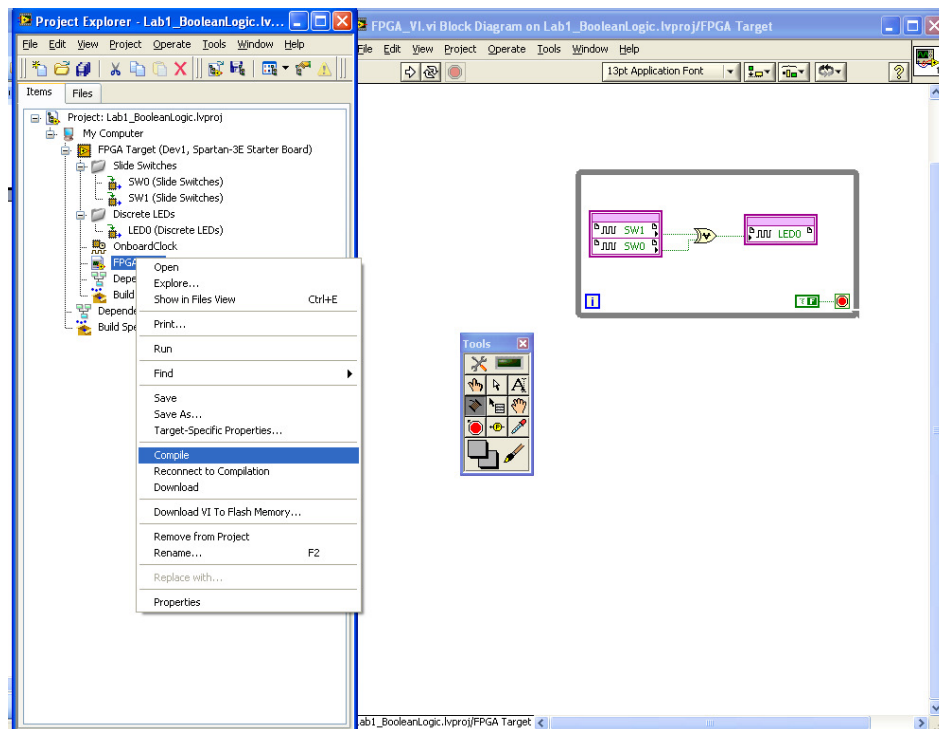


In this screen you see the option "Run when loaded to FPGA". Make sure you select this option. Then press the "OK" button.



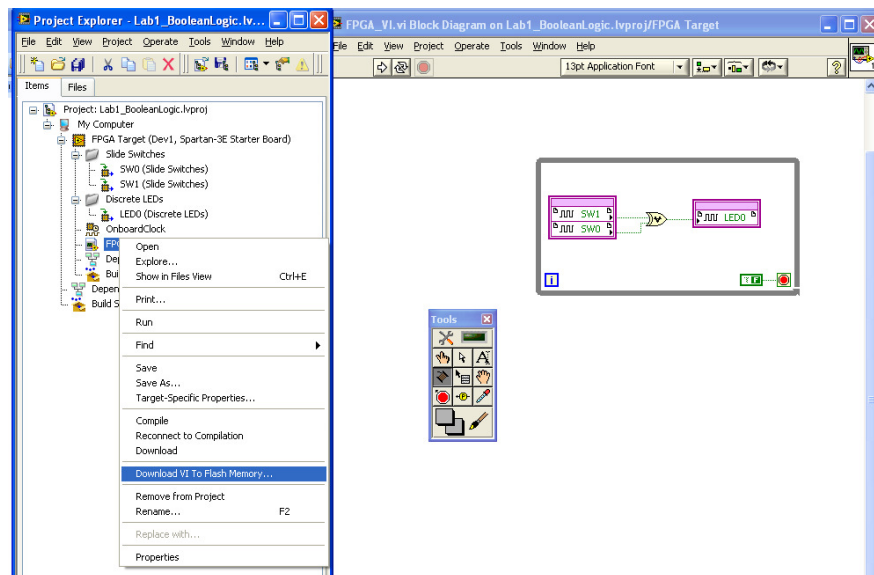


We must recompile the VI because we made a change. Do this by going to the “Project Explorer” view. Click with the “Right Mouse button” on the FPGA VI you have created for this project. Select the “Compile” option.

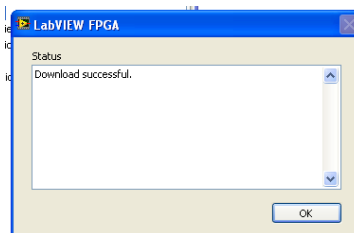


You will see that there are some previous explained steps executed. When the “Successful Compile Report” shows up you have to press the “OK” button. Now we will download it to the

Flash. For this you have to go to the “Project Explorer” view and do a “right mouse click” on the FPGA VI you created. Then choosing the “Download VI to Flash Memory” option will start downloading it to the Spartan-3E starter board flash.



When this box appears the LabVIEW FPGA VI is downloaded to the Flash.



Now you can pull out the USB cable out of the Xilinx Spartan3E board and press the PROG button on this board. You will see that the function is implemented in it.

Enjoy.

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